CLAIMS

1. A memory device comprising:

a delay-locked loop circuit having a plurality of delay elements;

a synchronization circuit coupled to said delay-locked loop circuit and a synchronization enable signal, said synchronization circuit outputting a plurality of enable signals; and

an output circuit having a buffer coupled to a data input enable signal and a data output enable signal, said buffer circuit generating an output.

2. The memory device of claim 1 wherein said delay-locked loop circuit receives an external clock signal.

3. The memory device of claim 1 further comprising a read circuit having a signal sense array.

4. The memory device of claim 3 wherein said synchronization circuit provides a first read enable signal to said read circuit.

5. The memory device of claim 3 wherein said synchronization circuit provides a second read enable signal to said read circuit.

6. The memory device of claim 1 wherein said output circuit further comprises a data input pointer and a data output pointer.

7. The memory device of claim 1 further comprising a data input pointer circuit coupled to receive said data input enable signal and a data output pointer circuit coupled to receive said data output enable signal.

8. The memory device of claim 7 further comprising a decoder coupled to receive an input pointer from said data input pointer circuit and generate an input address for said buffer.

9. The memory device of claim 8 wherein said decoder is further coupled to receive an output pointer from said data output pointer circuit and generate an output address for said buffer.

10. The memory device of claim 1 wherein said memory device comprises a dynamic random access memory.

11. A memory device comprising:

a delay-locked loop circuit having a plurality of delay elements;

a synchronization circuit coupled to said delay-locked loop circuit and a synchronization enable signal, said synchronization circuit outputting a plurality of enable signals; and

a read circuit having a signal sense amplifier coupled to said synchronization circuit, said read circuit receiving a read enable signal from said synchronization circuit.

12. The memory device of claim 11 further comprising an output circuit having a buffer coupled to said synchronization circuit.

13. The memory device of claim 12 wherein said output circuit further comprises a data input pointer circuit coupled to receive a data input enable signal and a data output pointer circuit coupled to receive a data output enable signal.

14. The memory device of claim 13 wherein said output circuit further comprises a decoder coupled to receive an input pointer from said data input pointer circuit and generate an input address for said buffer.

15. The memory device of claim 14 wherein said decoder is further coupled to an output pointer from said data output pointer circuit and generate an output address for said buffer.

16. A memory device comprising:

a delay-locked loop circuit having a plurality of delay elements, said delay-locked loop circuit generating a plurality of delayed clock signals;

a synchronization circuit coupled to said delay-locked loop circuit and receiving said plurality of delayed clock signals and a synchronization enable signal, said synchronization circuit outputting a data output enable signal; and

an output circuit having a buffer coupled to said synchronization circuit, said buffer circuit generating an output in response to said data output enable signal.

17. The memory device of claim 16 further comprising a read circuit having a signal sense amplifier coupled to said synchronization circuit, said read circuit receiving a read enable circuit from said synchronization circuit.

18. The memory device of claim 17 wherein said read enable circuit is based upon the synchronization enable signal and a delayed clock signal.

19. The memory device of claim 17 wherein said read circuit comprises a signal sense array coupled to a plurality of bit lines of said memory device.

20. A memory device comprising:

a delay-locked loop circuit having a plurality of delay elements, said delay-locked loop circuit generating a plurality of delayed clock signals;

a synchronization circuit coupled to said delay-locked loop circuit and receiving said plurality of delayed clock signals and a synchronization enable signal, said synchronization circuit outputting a plurality of enable signals;

a read circuit comprising a signal sense amplifier, said read circuit receiving a read enable signal; and

an output circuit coupled to said synchronization circuit, said output circuit receiving a data input enable signal enabling the storage of data in a buffer circuit and a data output enable signal enabling the output of data from said buffer circuit.

21. A method of reading data from a memory device, said method comprising:

coupling an external clock signal to a delay-locked loop circuit;

coupling a synchronization enable signal to a synchronization circuit;

generating a read signal based upon said synchronization enable signal and a first delayed clock signal of said external clock signal; and

synchronizing a data output enable signal to said read signal.

22. The method of claim 21 further comprising a step of generating a plurality of delayed clock signals based upon said external clock signal.

23. The method of claim 22 further comprising a step of generating a data input enable signal based upon said synchronization enable signal and a second delayed clock signal.

24. The method of claim 22 further comprising a step of generating a data output enable signal based upon said synchronization enable signal and third delayed clock signal.

25. The method of claim 22 wherein said step of generating a data output enable signal comprises a step of generating a data output enable signal which is synchronized to said read signal.

26. A method of reading data from a memory device, said method comprising:

coupling an external clock signal to a delay-locked loop circuit;

coupling a synchronization enable signal to a synchronization circuit;

generating a read signal based upon a synchronization enable signal and said external clock signal; and

generating a data output enable signal based upon said synchronization enable signal and said external clock.

27. The method of claim 26 further comprising a step of generating a plurality of delayed clock signals based upon said external clock signal.

28. The method of claim 26 further comprising a step of generating a data input enable signal based upon said synchronization enable signal and a second delayed clock signal.

29. The method of claim 26 wherein said step of generating a data output enable signal comprises generating a data output signal which is synchronized with said read signal.

30. The method of claim 26 further comprising a step of reading data from a dynamic random access memory.